IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A complementary metal oxide semiconductor (CMOS) semiconductor device, comprising:

a first gate electrode having a stacked structure of a first metal layer, a polysilicon layer and a second metal layer formed in a p-well region of a cell region and an n-well region of a peripheral circuit region; and

a second gate electrode having a stacked structure of the polysilicon layer and the second metal layer formed on a p-well of a peripheral circuit region.

2. (Original) The device of claim 1, wherein the first metal layer has a work function ranging from 4.8 eV to 5.0 eV.

3. (Original) The device of claim 1, wherein the first metal layer has a thickness ranging from 5 to 1000Å.

4. (Original) The device of claim 1, wherein the first metal layer comprises at least one metal layer selected from the group consisting of TiN, TiAlN, TiSiN, WN and TaN.

5. (Original) The device of claim 1, wherein the polysilicon layer have a thickness ranging from 10 to 1000Å.

6. (Original) The device of claim 1, wherein the second metal layer have a thickness ranging from 10 to 1000Å.

7-17. (Canceled)